

CLAIMS

3. A processing element as claimed in Claim 1, further including data bit-size indicator means.
5. A processing element as claimed in Claim 1, further including at least one register means.
9. A neural network controller as claimed in Claim 7, wherein the memory means includes buffer memory associated with said data input means and/or said data output means.
10. A neural network module (300) comprising an array of neural processing elements (100) as claimed in Claim 1; and at least one neural network controller (200) as claimed in Claim 7.
12. A modular neural network comprising:
one module (300) as claimed in Claim 10, or at least two modules (300) as claimed in Claim 10 coupled together.
13. A modular neural network as claimed in Claim 12, wherein the modules (300) are coupled in a lateral expansion mode and/or a hierarchical mode.
16. A modular neural network as claimed in claim 14, wherein the synchronisation means includes the use of a two-line handshake mechanism.
17. A neural network device comprising a neural network as claimed in Claim 12, wherein an array of processing elements (100) is implemented on the neural network device with at least one module controller (200).